REMARKS/ARGUMENTS

Claims 1-19 are pending. Claims 1-18 have been rejected. Claim 19 has been objected to. Claims 1 and 9 have been amended. Reconsideration is respectfully requested.

The drawings have been objected to because Figures 7-10 are not designated by a legend such as prior art. Submitted herewith is a letter to the chief draftsperson enclosing new formal drawings Figure 7-10 labeled as prior art. A copy of Figures 7-10 are attached to this amendment as an appendix for the convenience of the examiner. Withdrawal of the objection to the drawings is requested.

Claim 19 has been objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form. The allowable subject matter of Claim 19 is noted. It is respectfully submitted that Claims 17-18 from which Claim 19 depends directly and indirectly are allowable for the reasons described below, and thus claim 19 need not be rewritten in independent form. Therefore, withdrawal of the objection to Claim 19 is respectfully requested.

Claims 1-18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Won et al.* (U.S. Patent No. 6,216,240) in view of *Duesman* (U.S. Patent No. 6,169,695).

Claim 1 has been amended merely to further define the invention and recites in pertinent part "said formality of DRAM circuits are cyclically accessed for each row."

It is asserted in the Office Action that *Won* teaches a plurality of DRAM circuits (FIG. 1), a control circuit that receives a test control signal to perform a test control in which the RAM circuits are tested (FIG. 2), an input selector that is controlled by the control circuit and inputs a DRAM macro signal to the DRAM circuitry at the time of the test (FIG. 3), and an output selector that is controlled by the control circuit and outputs signals of the DRAM circuitry at the time of the test (FIG. 4).

Applicants traverse this rejection for the reasons as set forth below.

Although the Office Action is not specific, it appears that the first multiplexer 45a and the second multiplexer 45b of FIG. 4 of *Won* are asserted to correspond to the output selector recited

in Claim 1. It is respectfully submitted that the multiplexers 45a and 45b are not the output selector recited in Claim 1, which recites "an output selector that is controlled by said control circuit, and output signals of said plurality of DRAM circuits sequentially to a macro output terminal at the time of test." In contrast to the output selector of Claim 1, the first and second multiplexers 45a and 45b of *Won* output signals to first and second memories, and does not output signals to an output terminal as recited in Claim 1. Specifically, *Won* describes the first multiplexer 45a transmitting signals generated from the first AND gate 43a to the first memory 17 of FIG. 1 (columns 7, lines 6-8). Similarly, *Won* further describes the second multiplexer 45b transmitting signals generated from the third AND gate 43c to the second memory 19 of FIG. 1 (column 7, lines 19-21). Hence, *Won* does not disclose or even suggest the claimed feature of "an output selector . . . outputs signals . . . to a macro output terminal." Lacking at least this claim feature, *Won* cannot render Claim 1 unpatentable.

As conceded in the Office Action, *Won* does not disclose a methodology of testing the DRAM circuits. *Duesman* is cited for disclosing a methodology of testing DRAM circuits.

Amended claim 1 recites "a control circuit that receives a test control signal to perform a test control in which said plurality of RAM circuits are tested while the access to said plurality of DRAM circuits is subsequently changed for each row and said plurality of DRAM circuits are cyclically accessed for each row." As understood, *Duesman* merely discloses a row access sequence of one DRAM, and does not disclose or even suggest the "said plurality of DRAM circuits are cyclically accessed for each row" of the control circuit recited in amended claim 1. Lacking at least this claim feature, *Duesman* cannot render Claim 1 unpatentable.

The combination of *Won* and *Duesman* at best merely discloses a methodology of testing the DRAM circuits of the system of *Won*. Thus, for the foregoing reasons, the combination of *Won* and *Duesman* does not disclose or even suggest the output selector or the plurality of DRAM circuits cyclically addressed for each row as recited in Claim 1. Therefore, neither *Won* nor *Duesman* either individually or in combination render Claim 1 unpatentable. Because Claims 2-8 depends indirectly on Claim 1, for similar reasons Claims 2-8 are patentable over the

combination of *Won* and *Duesman*. Therefore, it is respectfully submitted that Claims 1-8 are patentable over the references of record.

Claim 9 has been amended merely to correct a typographical error.

It is asserted in the Office Action that *Won* teaches a plurality of DRAM circuits (FIG. 1), a plurality of control circuits corresponding to a DRAM circuit, that receive a test control signal to perform a test control in which the DRAM circuits are tested (FIG. 2); and an output selector that is controlled by a control circuit signal and outputs signals of the DRAM circuitry at the time of the test to an output terminal (FIG. 4).

Applicants traverse this rejection for the reasons as set forth below.

Although the Office Action is not specific, it appears that the controllers 25 and 27 of FIG. 2 of *Won* are asserted to be the plurality of control circuits recited in claim 9. It is respectfully submitted that the controllers 25 and 27 are not the control circuits recited in claim 9, which recites "a plurality of control circuits each of which . . . receives a test control signal to perform a test control of said corresponding one DRAM circuit." In the circuit of FIG. 2 of *Won*, the controller 25 is a memory control signal controller to perform a test control. However, the controller 27 is not a memory control signal controller but a memory data controller for controlling data. In fact, as shown in FIG. 2 of *Won*, an output signal of the memory control signal controller 25 is inputted to the first and second memories. That is, the memory control signal controller 25 is used for controlling not only the first memory but also the second memory for memory control. The controller 27 is a memory data controller. Thus, the controllers 25 and 27 of *Won* are not the control circuits recited in claim 9.

Hence, *Won* does not disclose or even suggest "a plurality of control circuits each of which . . . receives a test control signal to perform a test control of said corresponding one DRAM circuit" as recited in claim 9.

Furthermore, the multiplexer 45a and 45b (FIG. 4 of Won) are not the output selector of claim 9 for similar reasons as noted above in conjunction with claim 1. Hence, *Won* does not disclose or even suggest the output selector recited in claim 9.

The Office Action is silent as to how *Duesman* is applied to claim 9. *Duesman* is cited against claim 1 for disclosing a methodology of testing DRAM circuits. *Duesman* does not disclose or even suggest the control circuits or the output selector recited in claim 9. The combination of *Won* and *Duesman* does not disclose or even suggest the control circuits or the output selector recited in claim 9. Lacking at least these claim features, neither *Won* nor *Duesman*, either individually or in combination, can render claim 9 unpatentable. For similar reasons, neither *Won* nor *Duesman*, either individually or in combination, can render claims 10-16, which depend directly or indirectly on claim 9, unpatentable. Therefore, it is respectfully submitted that claims 9-16 are patentable over the references of record.

Referring now to claim 17, it is asserted in the Office Action that *Won* discloses a plurality of DRAM circuits (FIG. 1), a control circuitry that receive a test control signal and controls the DRAM circuitry simultaneously and independently (FIG. 2, 3), and input selector that inputs a DRAM macro signal to the DRAM circuitry at the time of the test (FIG. 3), and an output selector that outputs signals of the DRAM circuitry at the time of the test to an output terminal (FIG. 4).

Applicants traverse this rejection for similar reasons as presented above against the rejection of claim 1.

Although the Office Action is not specific, it appears that the first multiplexer 45a and the second multiplexer 45b of FIG. 4 of *Won* are asserted to be an output selector corresponding to the output selector recited in claim 17. It is respectfully submitted that the multiplexers 45a and 45b are not the output selector recited in claim 17, which recites "an output selector . . . outputs signals of the plurality of DRAM circuits . . . to a macro output terminal." In contrast to the output selector of claim 17, the first and second multiplexers 45a and 45b of *Won* output signals to first and second memories, and does not output signals to an macro output terminal as recited in claim 17. Lacking at least this claim feature, *Won* cannot render claim 17 unpatentable. *Duesman* is applied for disclosing accessing DRAM circuits sequentially and transferring the information to outside the DRAM circuitry. However, *Duesman* does not disclose or even

suggest "an output selector . . . output signals from the plurality of DRAM circuits . . . to a macro output terminal" as recited in claim 17. Lacking at least this claim feature, *Duesman* cannot render claim 17 unpatentable. The combination of *Won* and *Duesman* at best merely discloses a methodology of testing the DRAM circuits in the system of *Won*. Thus, for the foregoing reasons, the combination and *Won* and *Duesman* does not disclose or even suggest the output selector recited in claim 17. Therefore, neither *Won* nor *Duesman*, either individually or in combination, render claim 17 unpatentable. Because claim 18 depends on claim 17, for similar reasons, the combination of *Won* and *Duesman* cannot render claim 18 unpatentable. Therefore it is respectfully submitted that claims 17-18 are patentable over the references of record.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

The Commissioner is hereby authorized to charge any fees which may be required, or credit in the overpayment, to Deposit Account No. 07-1896 referencing Attorney Docket No. **2102475-991110**.

Respectfully submitted,

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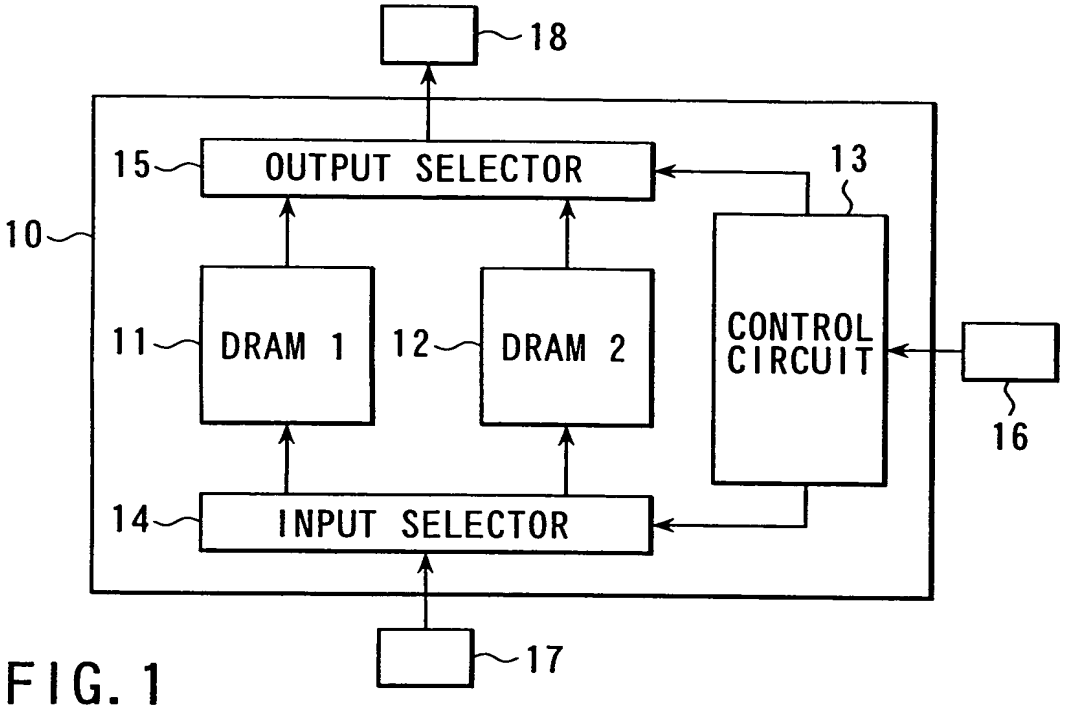


FIG. 1

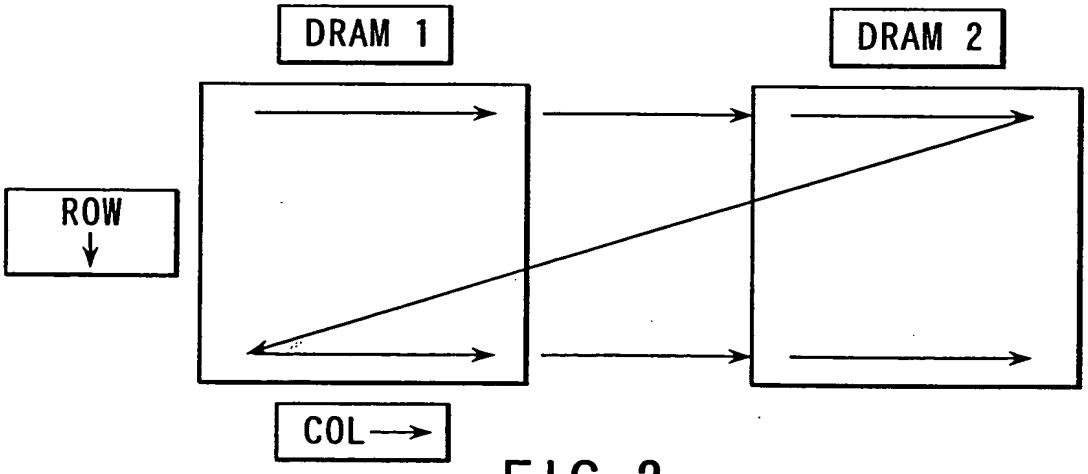


FIG. 2

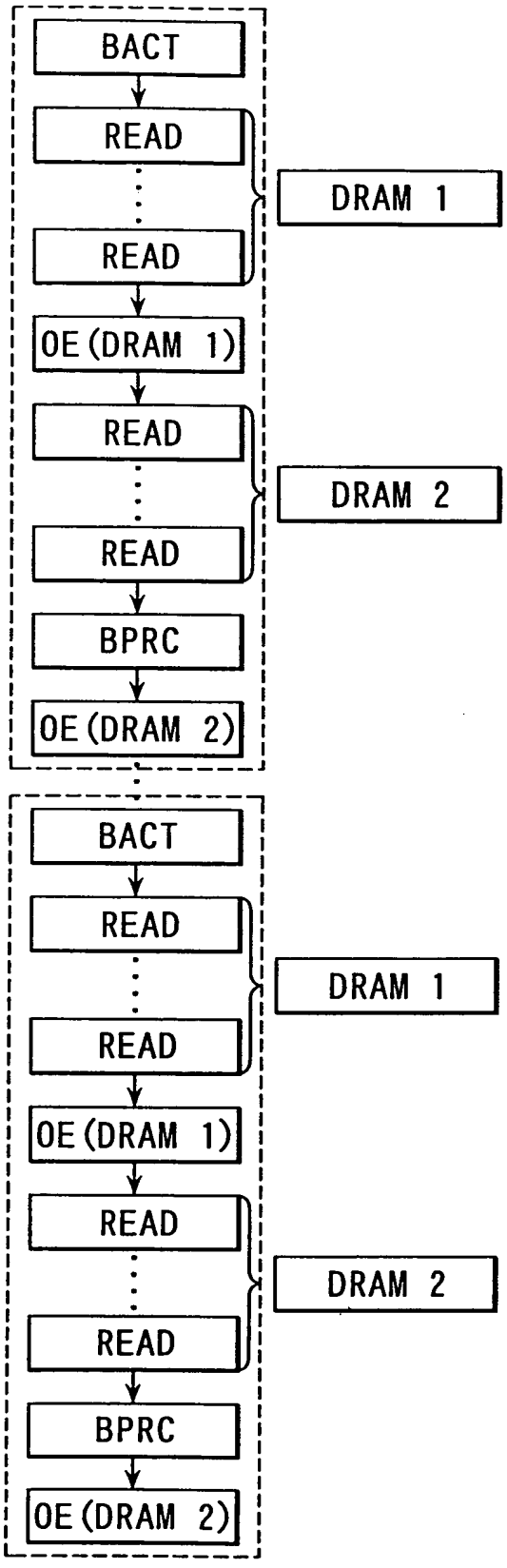


FIG. 3

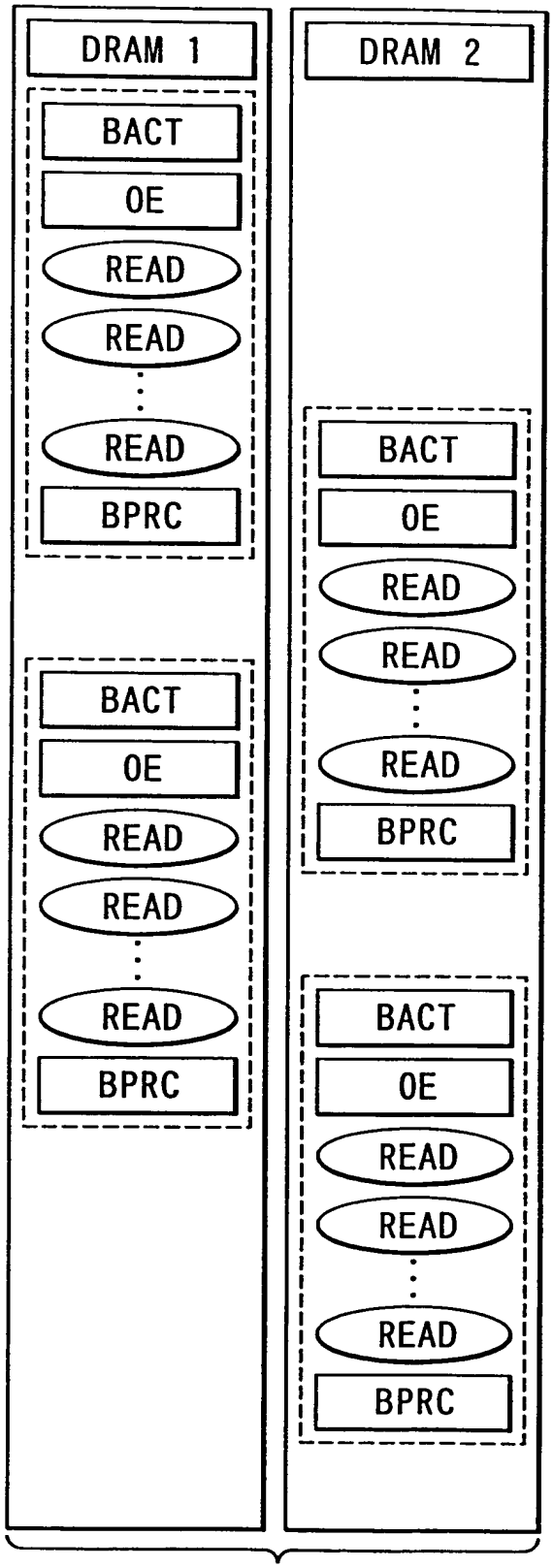


FIG. 6

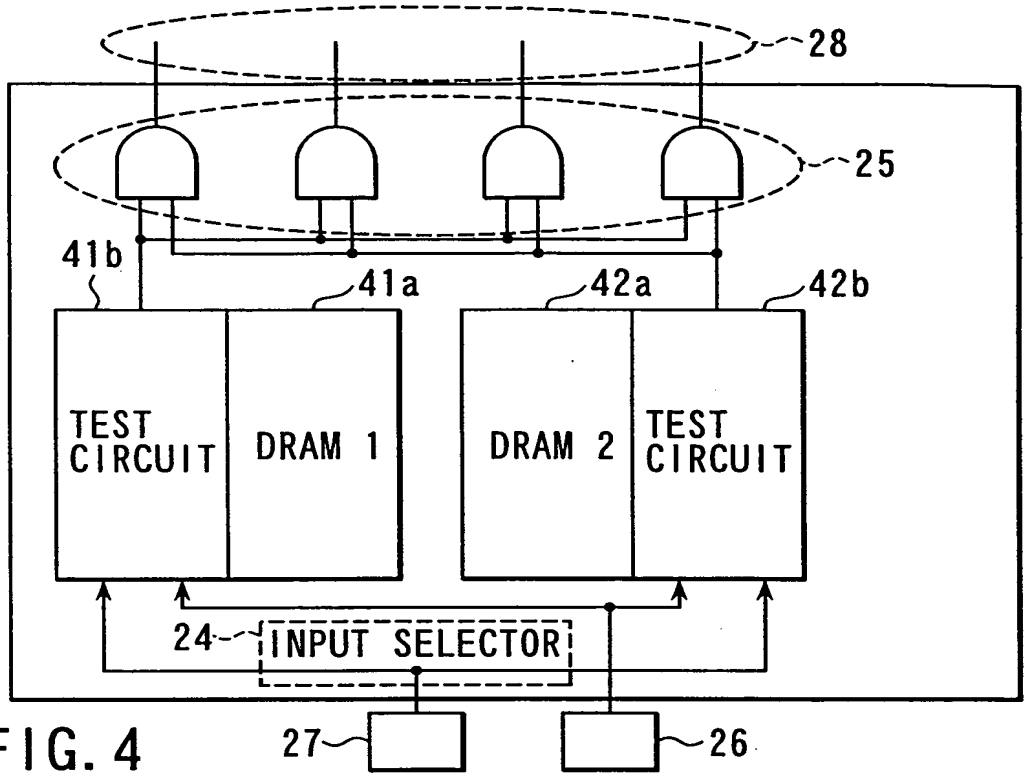


FIG. 4

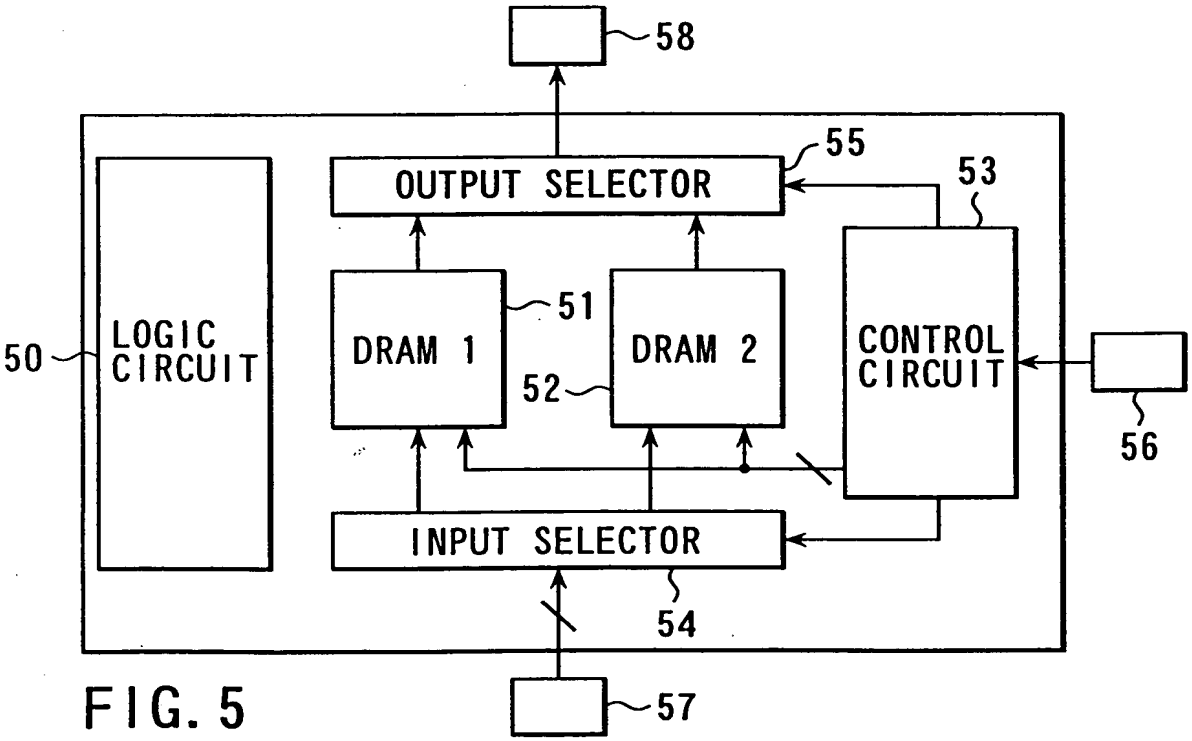
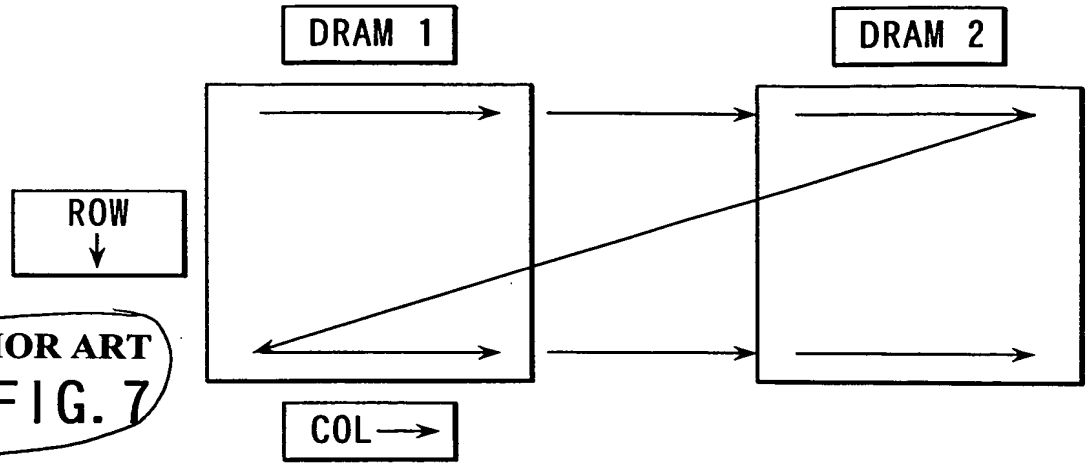
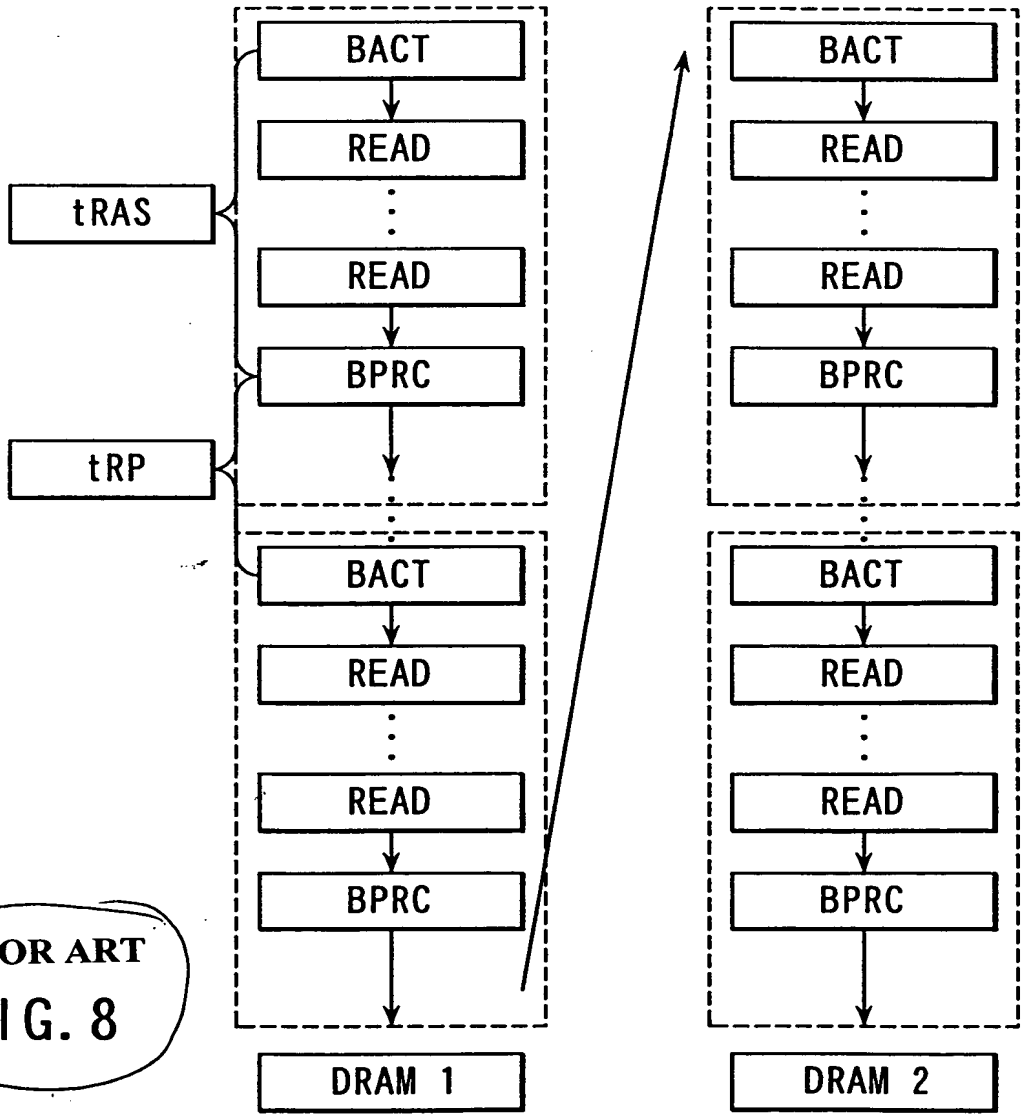


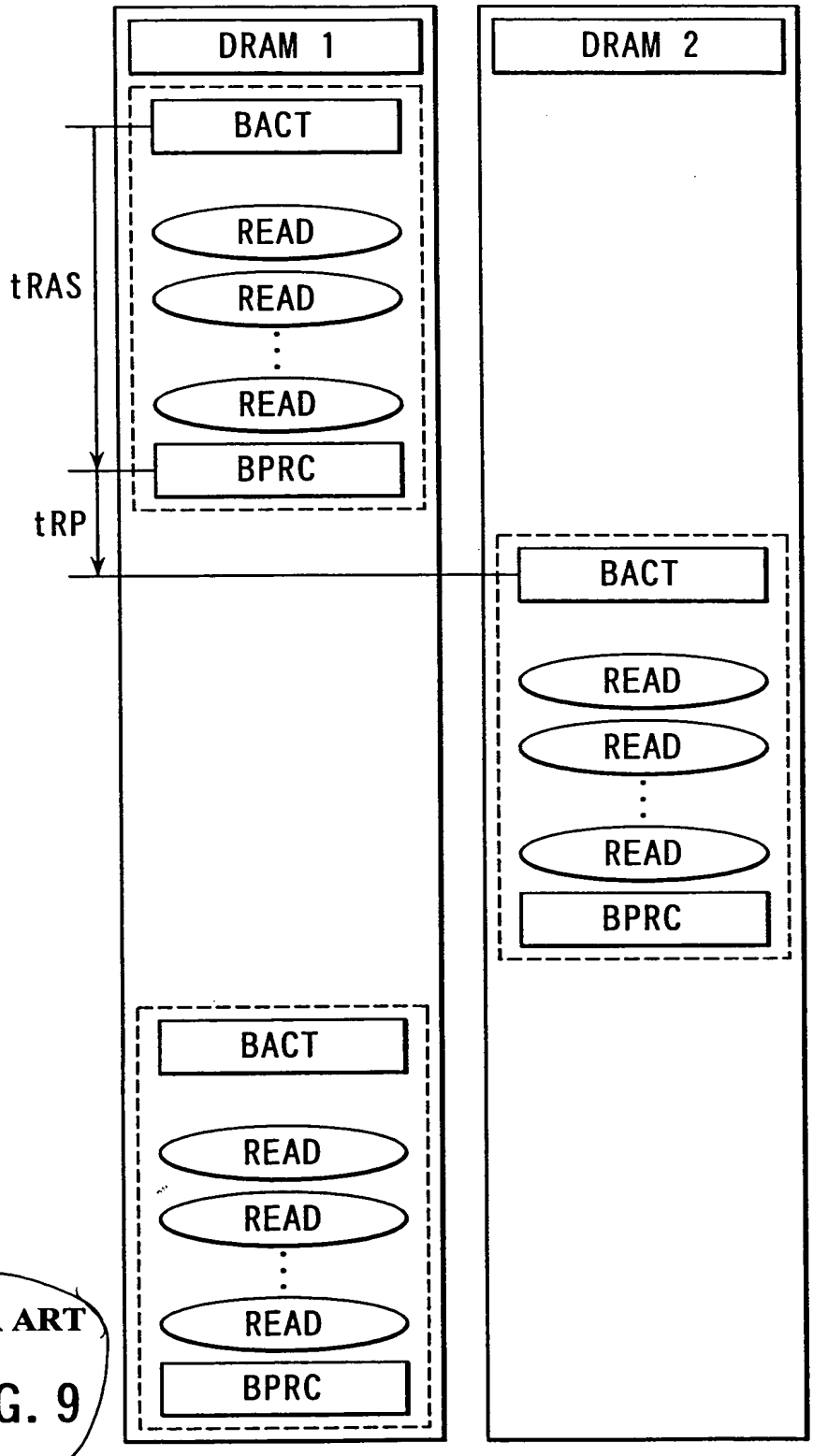
FIG. 5



PRIOR ART
FIG. 7

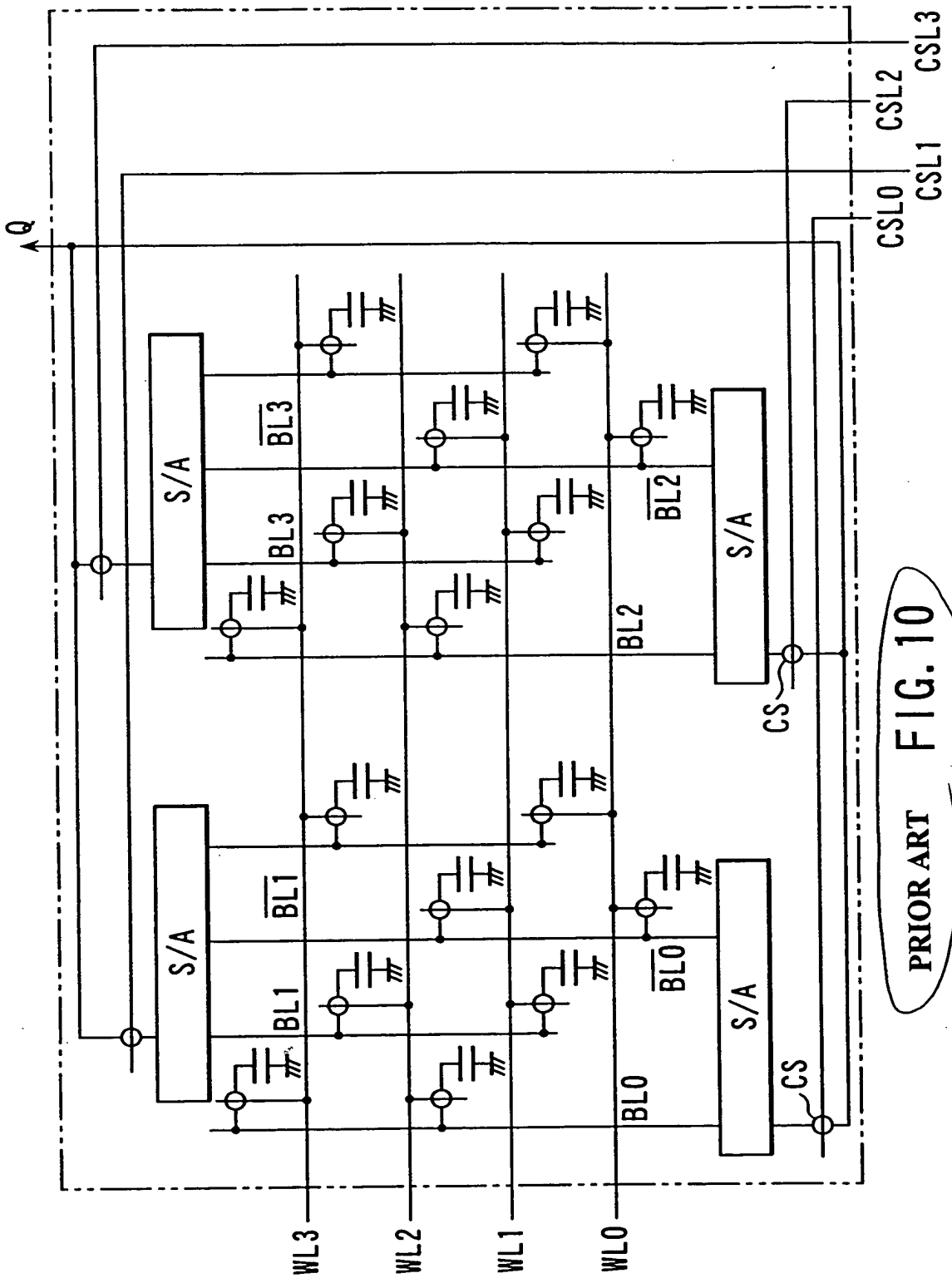


PRIOR ART
FIG. 8



PRIOR ART

FIG. 9



PRIOR ART FIG. 10